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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,215	07/31/2003	Gerard Chauvel	TI-35460	1111

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EXAMINER	
AHMED, HAMDY S	

ART UNIT	PAPER NUMBER
2188	

NOTIFICATION DATE	DELIVERY MODE
02/15/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/632,215	CHAUVEL, GERARD	
	Examiner	Art Unit	
	Hamdy S. Ahmed	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- 10 and 12-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Lehman et al (US No: 5,680,161).

As to claim 1, Lehman discloses a system comprising: a processor executing an application; a peripheral device coupled to the processor; memory containing an application data structure accessible by said application (see figure 3, where the host computer is connected to a processor that is connected to the memory where the data structure is, and also connected to peripheral device, which is the monitor), wherein accesses to said application data structure and accesses to said device are formatted differently (see abstract, lines 1 - 6), and wherein data can be written to, or read from, the peripheral device via the application data structure (for r/w operations, see figure 5, the data has always been written and read via a peripheral device such as a keyboard and display device such as a monitor); and reformat logic coupled to the processor and memory, the reformat logic dynamically reformats an access from the application targeting the application data structure to a format that comports with the device (see figure 3, where the logic device element 26 is connected to the host processor element 20 and accesses the memory (25) ,and the result will be displayed), thereby permitting said application to manage the peripheral device without the use of a device driver (see column 3, lines 52- 55, the procedure is done without a driver); wherein the reformat logic includes alignment logic that implements a read-modify-write operation to write a value from the

operation data structure across byte boundaries in the display buffer (the logic device reformat the into pixels and change the data into red, green and blue to be written and displayed, see column 7, lines 28-49).

As to claim 2, Lehman discloses wherein the peripheral device comprises a display (see figure 3, element 30).

As to claim 3, Lehman discloses wherein the application data structure comprises an array (see column 3, lines 24-25).

As to claim 4, Lehman discloses wherein the array comprises a multi-dimensional array (inherently the array of pixels comprises a multi-dimensional see column 4, line 53).

AS to claim 5 Lehman discloses wherein array comprises a single-dimensional array (the array that comprises pixel of one is a single-dimensional see column 4,lines 45-53).

As to claims 6 and 16, Lehman discloses further including a device buffer associated with the device and wherein the application data structure comprises an n-bit data structure and the device buffer comprises an m-bit display buffer (32-bit video data is compressed into 24-bit color pixels, where n is 32 and m is 24, see column 3, lines 35 - 38), wherein n is different than m, and the reformat logic reformats an n-bit access from the application to an m-bit access for the device buffer (the graphics controller contains circuitry for reformatting host data words into a format that is suited to dense packing in video memory, see column 3, lines 44 - 54).

As to claim 7, Lehman discloses wherein n is not an integer multiple of m (32-bit video data is compressed into 24-bit color pixels, where n is 32 and m is 24, see column 3, lines 35 - 38)

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As to claim 8, Lehman discloses wherein m is less than n (32-bit video data is compressed into 24-bit color pixels, where n is 32 and m is 24, see column 3, lines 35 - 38).

As to claim 9, Lehman discloses wherein the reformat logic comprises a plurality of

registers which are programmable to store a plurality of values (both shift and output registers are used to store data, see column 3, lines 55 - 63), said values comprising information that is indicative of the starting and ending addresses of the application data structure in which accesses are to be reformatted by the reformat logic, the starting address of the device buffer, n, and m (the video display contains pixels that are arranged such that each is mapped sequentially to internal video memory addresses, each of which is associated with a portion of a memory location, see column 3, lines 55 - 67, and column 4, lines 1-3).

As to claim 10, Lehman discloses wherein the reformat logic comprises a plurality of registers which are programmable to store a plurality of values (both shift and output registers are used to store data, see column 3, lines 55 - 63), said values comprising information that is indicative of the starting and ending addresses of the application data structure in which accesses are to be reformatted by the reformat logic (the video display contains pixels that are arranged such that each is mapped sequentially to internal video memory addresses, each of which is associated with a portion of a memory location, see column 3, lines 55 - 67, and column 4, lines 1-3), the starting address of the device buffer, n, and value indicative of the ratio between n and m (the 24-bit pixels are divided so that they are in a 32-bit format for storage in a memory location, see column 3, lines 42 - 50).

As to claim 12, Lehman discloses further comprising a multiplexer that selectively permits accesses from the application to be provided to bypass the reformat logic so that such accesses are not reformatted by the logic (the graphic controller receives the video data over bus and without reformatting process this data, see column 8, lines 21-34) and permits accesses from the application to be reformatted before being provided to the memory (see column 12, lines 57 - 64).

As to claim 13, Lehman discloses wherein the reformat logic controls the multiplexer to

select whether or not a reformatted access is to be provided to the memory (the multiplexer is to select a pixel from the pixel data, see column 12, lines 57-60).

As to claim 14, Lehman discloses wherein the processor supplies an address to the multiplexer and to the reformat logic and asserts a signal to the multiplexer to cause the multiplexer to select whether or not a reformatted access is to be provided to the memory (the processor sends the signal to the multiplexer to select a pixel from the pixel data, see column 12, lines 57 - 64).

As to claim 15, Lehman discloses reformat logic, comprising: a plurality of registers (both shift and output registers are used to store data, see column 3, lines 55 - 63); and translation logic that accesses the registers and that receives a memory access targeting an application data structure that has a different format than for accesses that are provided to a device that is external to said reformat logic and that reformats the request to a format compatible with the device based on values stored in the registers (see abstract, column 3, lines 19-67, and column 11, lines 40 - 45); wherein the translation logic implements a read-modify-write operation to write a value from the application data structure across byte boundaries of a memory buffer associated with said device (the logic device reformatting the 32 bit word the into 24 bits pixels and change the data into red, green and blue to be written and displayed, and this procedure is equivalent to the logic translation see column 7, lines 28-49).

As to claim 17, Lehman discloses wherein n is not an integer multiple of m and the reformat logic includes alignment logic to implement the read-modify-write operation (see column 7, lines 50 - 65).

As to claims 18 and 19 Lehman discloses further comprising a plurality of registers which are configured to be programmed to store a plurality of values (see column figure 9, where large number of bits stored in the register), said values comprising values that enable to

determine the starting and ending addresses of the application data structure in which accesses are to be reformatted by the reformat logic, the starting address of the memory buffer, n, and m (see column 3, lines 18 - 50).

As to claim 20 wherein the translation logic reformats both read and write requests (see column 11, lines 37- 47).

As to claim 21, Lehman discloses wherein the memory buffer for which the reformat logic reformats a request comprises a display memory buffer associated with a display (see abstract, lines 1 - 8).

As to claim 22, Lehman discloses a method, comprising: receiving a physical address from a processor, the physical address associated with an application data structure (the processor sends the signal to the multiplexer to select a pixel from the pixel data, see column 12, lines 57 - 64), converting the physical address to a device buffer address associated with a device buffer, the device buffer being accessed with a different number of bits than the application data structure; and providing the converted device buffer address to the device buffer (the graphics controller contains circuitry for reformatting host data words into a format that is suited to dense packing in video memory, see column 3, lines 44 - 54) to permit the processor to control a peripheral device without using a driver associated with the peripheral device (see column 3, lines 18 - 23), and perform a read-modify-write operation to write a value from the operation data structure across byte boundaries in the display buffer (the logic device reformat the into pixels and change the data into red, green and blue to be written and displayed, see column 7, lines 28-49).

As to claim 23, Lehman discloses wherein receiving the physical address from the processor is performed upon writing to the application data structure (inherently the processor is responsible for determining the address of the location to which the data is to be written).

As to claim 24, Lehman discloses wherein receiving the physical address from the processor is performed upon reading from the application data structure (the job of the processor is to determine the address of the data structure in order for the process of reading to be completed, see column 10, lines 34 - 45).

As to claim 25, Lehman discloses further including completing a read or write transaction to the device buffer using the converted device buffer address (see column 3, lines 18 – 34).

As to claim 26, Lehman discloses wherein the device buffer is accessed with fewer bits than the application data structure (the data is compressed from 32-bit video data to 24-bit color pixels, see column 3, lines 18 – 34).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 and is rejected under 35 U.S.C. 103(a) as being unpatentable over Lehman (US No: 5,680,161) in view Huber et al. (US No: 6,070,173).

As to claims 11 Lehman reference teaches all the limitation of claim 1 as the above, but Lehman reference does not teach, wherein the registers are programmed by virtual machine. The Huber reference teaches wherein the registers are programmed by virtual machine (see column 6, lines 5-14). Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the Lehman system by using the Huber system reference and used registers that are

programmed by virtual machine in order to determine the range of virtual addresses to be assigned to the Java object.

Response to the argument

With regard to the first argument, Lehman discloses a write operation (where the graphic control the writing of 24 bits see column 8, lines 21-34). With respect to the second argument, Lehman discloses, a read-modify-write operation (the logic device reformat the into pixels and change the data into red, green and blue to be written and displayed, any change happened in this process is modification see column 7, lines 28-49). With regard to the forth argument, Lehman discloses updating of just one 8 bit color value at a given 32- bits memory address (see column 5, lines 29—45). With regard to fifth argument, Lehman discloses, a storage device to store the claimed value (if the value stored in a register or stored in buffer there is no different both are storage elements, see column 8, lines 35-55).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hamdy S. Ahmed whose telephone number is 571-270-1027. The examiner can normally be reached on M-TR 7:30-5:00pm and Every 2nd Friday 7:30-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HA
Hamdy Ahmed
2/11/08

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02/12/08